Technische Universität Kaiserslautern

Institute of
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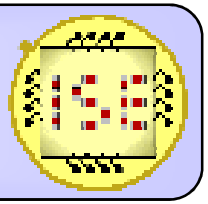
Dept. of Electrical Engineering and Information Technology

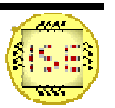


Design of a Wide Dynamic Range Active Pixel Sensor using Self-Reset Technique

Kai Lutz

November 2009

Project for the HEIS Lecture
of Prof. Dr.-Ing. Andreas König



Overview

I. Introduction
   1. *Motivation*
   2. *Dynamic Range*
   3. *Goals*

II. Parts of the Project
   1. *Self-Reset Technique*
   2. *The Comparator*
   3. *Counter using toggle-FF's*
   4. *4T DRAM Memory*
   5. *Layout*
   6. *Simulation Results*

III. Conclusion *and Future Work*

IV. Bibliography

1.Motivation

- Market for solid-state image sensors is rapidly growing.
- CCD vs. CMOS(PPS,APS or DPS).
- CMOS advantage: Integrating of sensing, analog and digital processing directly on the pixel.
  - Manufacturing with existing technology.
  - Less expensive.
  - Non-destructive readout (APS,DPS).
  - Following the CMOS scaling trend.
- Applications:
  - Consumer electronics (Digicams/Mobile Phones).
  - Machine vision.
  - Biological testing.
  - …etc.

2.Dynamic Range

- Relation of brightest to darkest picture areas.
- Typical CMOS image sensors Dynamic Range ≈ 60dB.
- Full range of real world‘s illumination ≈ 100dB.

⇒ More or less specifics will be lost.

⇒ Sensor with higher DR will produce higher quality pictures.

3.Goals

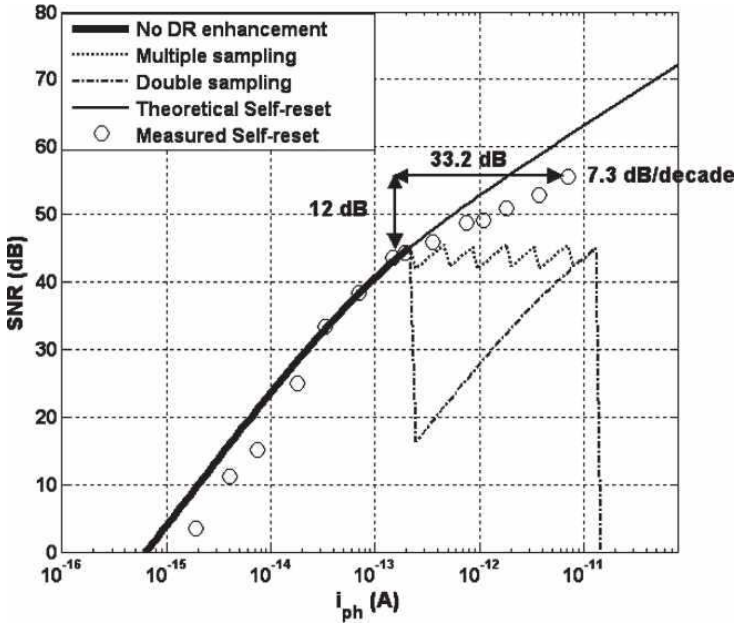
- Compare different techniques to increase DR and SNR of an Active Pixel Sensors.
  → DR synonymous to sensor quality.
- Choose the one that is most promising and functional.
- Implement the technique on a pixel cell in 0.35µm tech.
- Consider possibilities to reduce error-proneness (FPN etc.)
- Discuss the results.

2.Dynamic Range

How to increase the DR?

Techniques to increase DR at the high end [1][2]
=> increasing $i_{\max}$ or $Q_{\max}$.

1. Varying integration time:
   - Shuttering.
   - Well-capacity Adjusting (spiking).
   - Time to saturation.
   - Multiple-capture.
2. Recycling the well using self-resetting:
   - Time discrete or continuous monitoring.
   - Synchronous or asynchronous reset.
   - Will also increase peak SNR performance (high end).

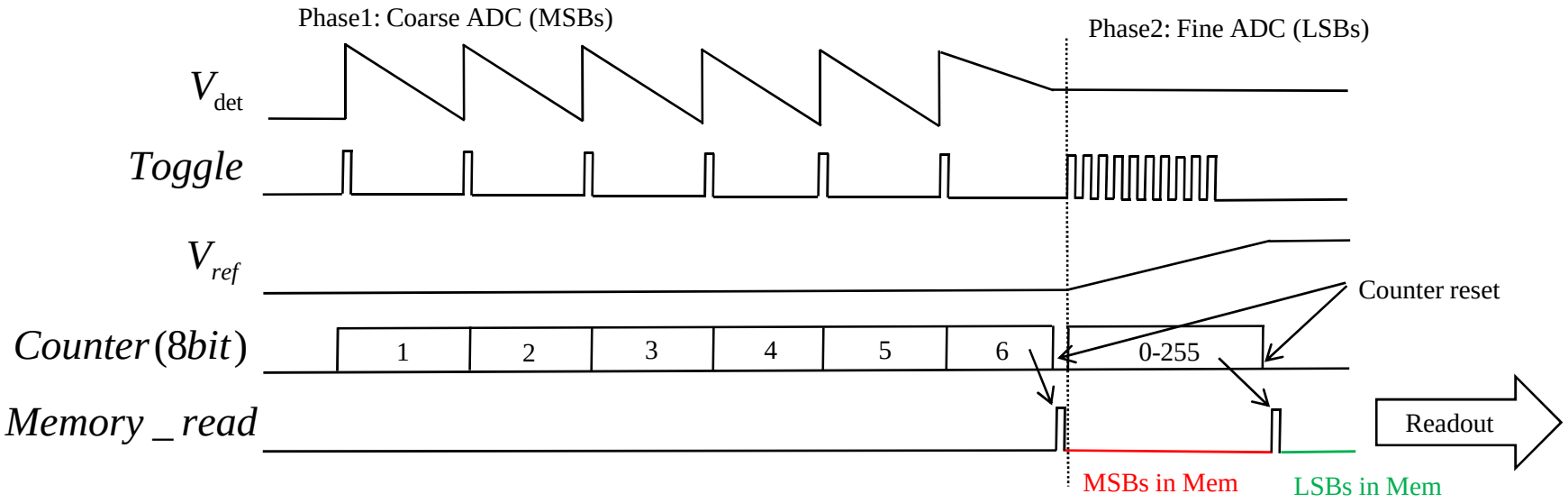


$$DR = \frac{i_{\max}}{i_{\min}} \approx \frac{Q_{\max}}{\sigma_{readout}}$$

$$SNR_{peak} = \frac{Q_{\max}}{q}$$

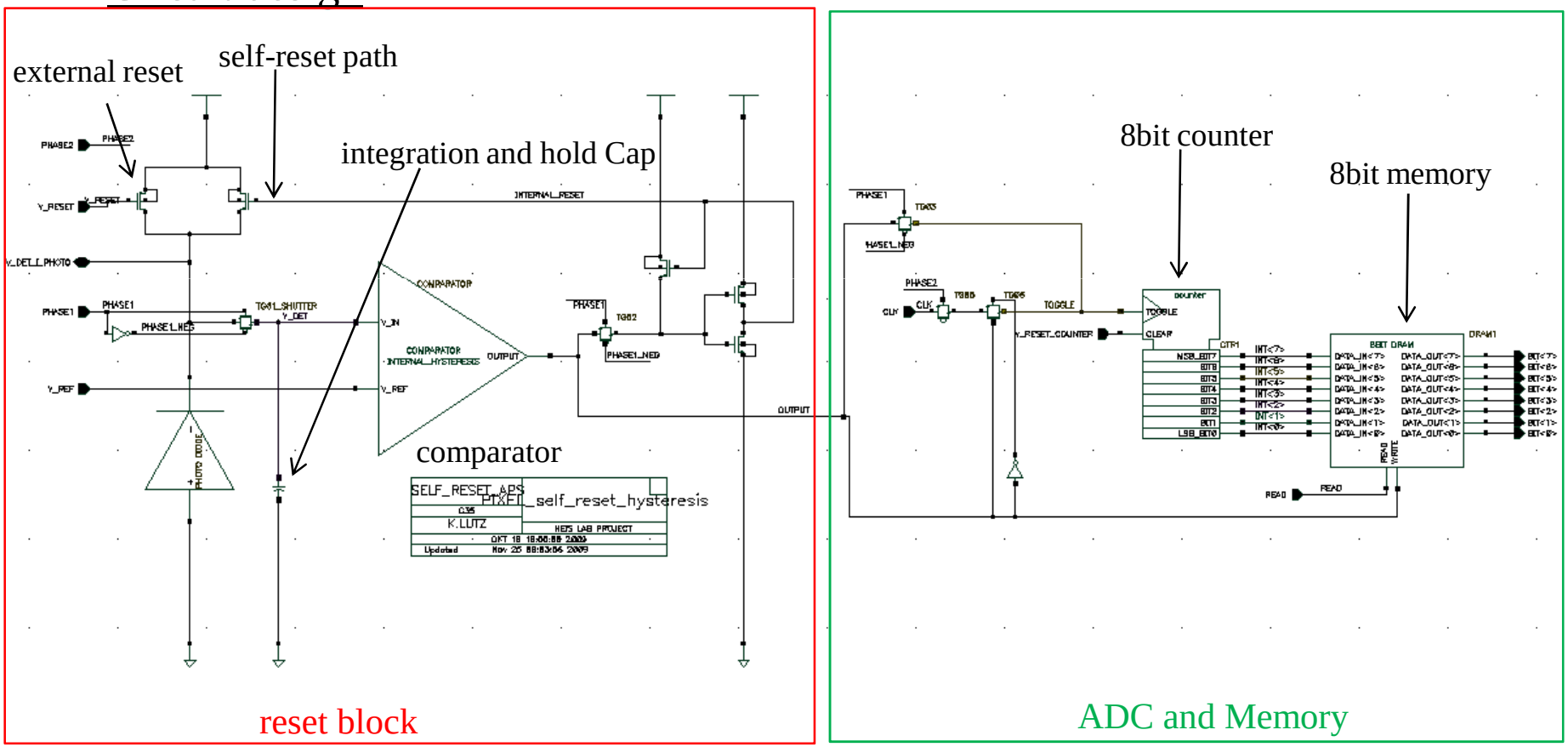
1. Self-Reset Technique

- Idea of self-reset pixel presented by Rhee and Joo[4][5].
- 2 Phases: Fine and coarse A/D conversion (counter and single slope ADC).
- Asynchronous well reset (increase effective well capacitance) .
- 8 bit DRAM to store MSBs for readout during phase 2.
- Pixel parallel ADC.



1. Self-Reset Technique

Circuit design

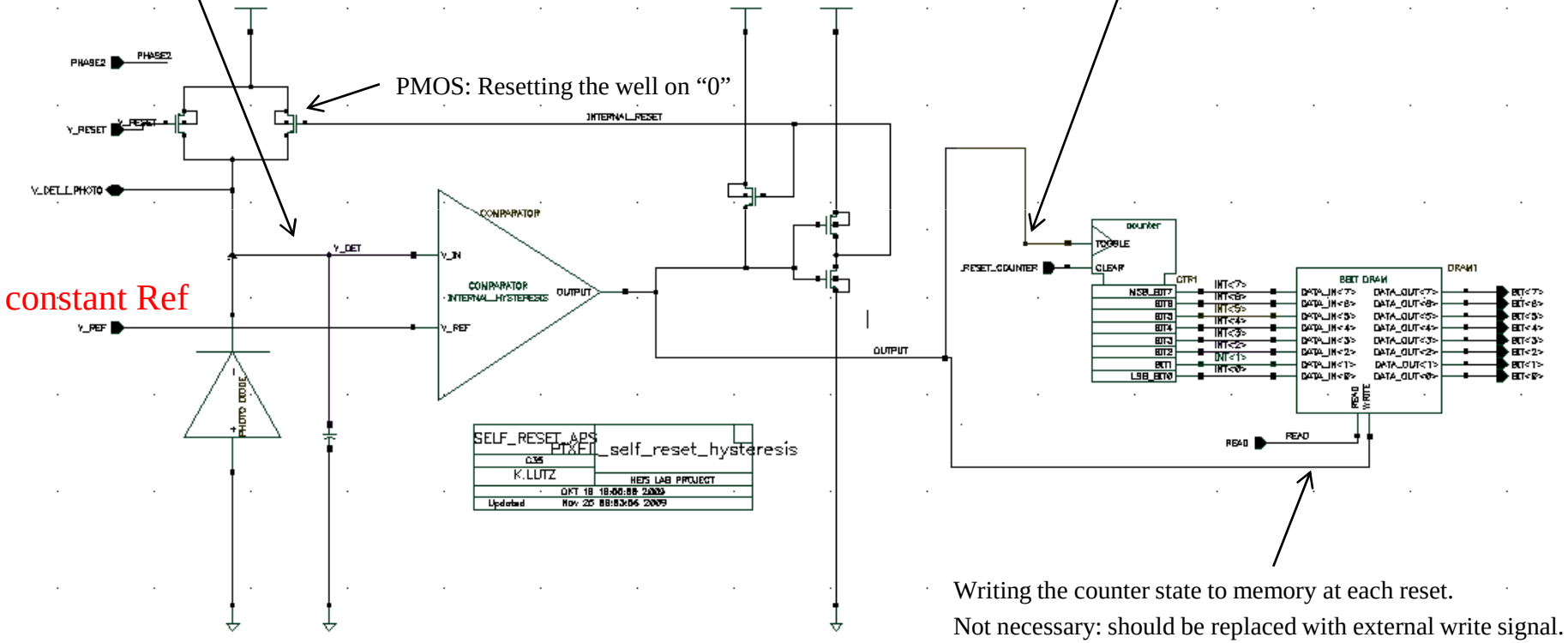


1. Self-Reset Technique

Phase 1

Integration

Counting the resets: “1” on the comparator output



Writing the counter state to memory at each reset.

Not necessary: should be replaced with external write signal.

1. Self-Reset Technique

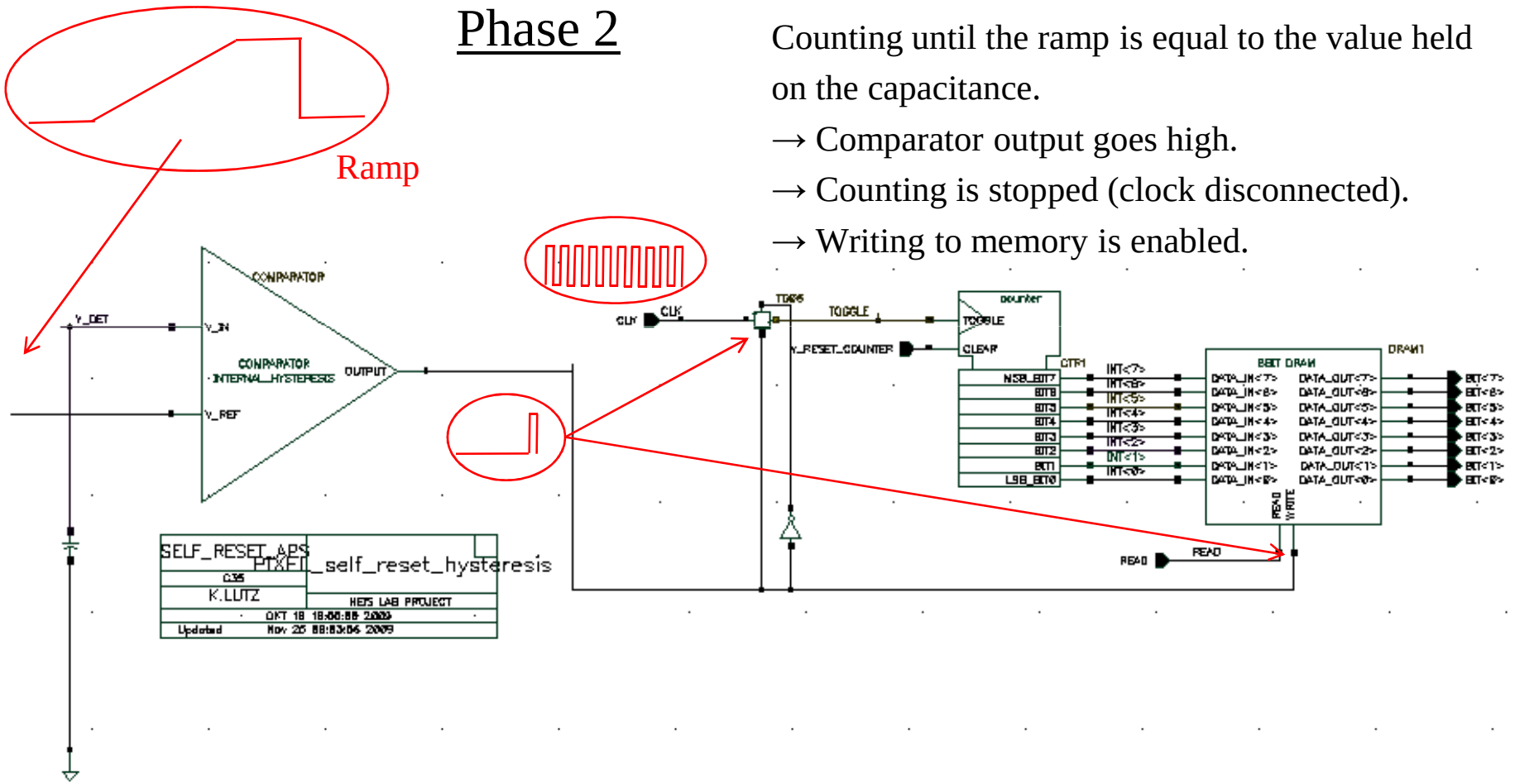
Phase 2

Counting until the ramp is equal to the value held on the capacitance.

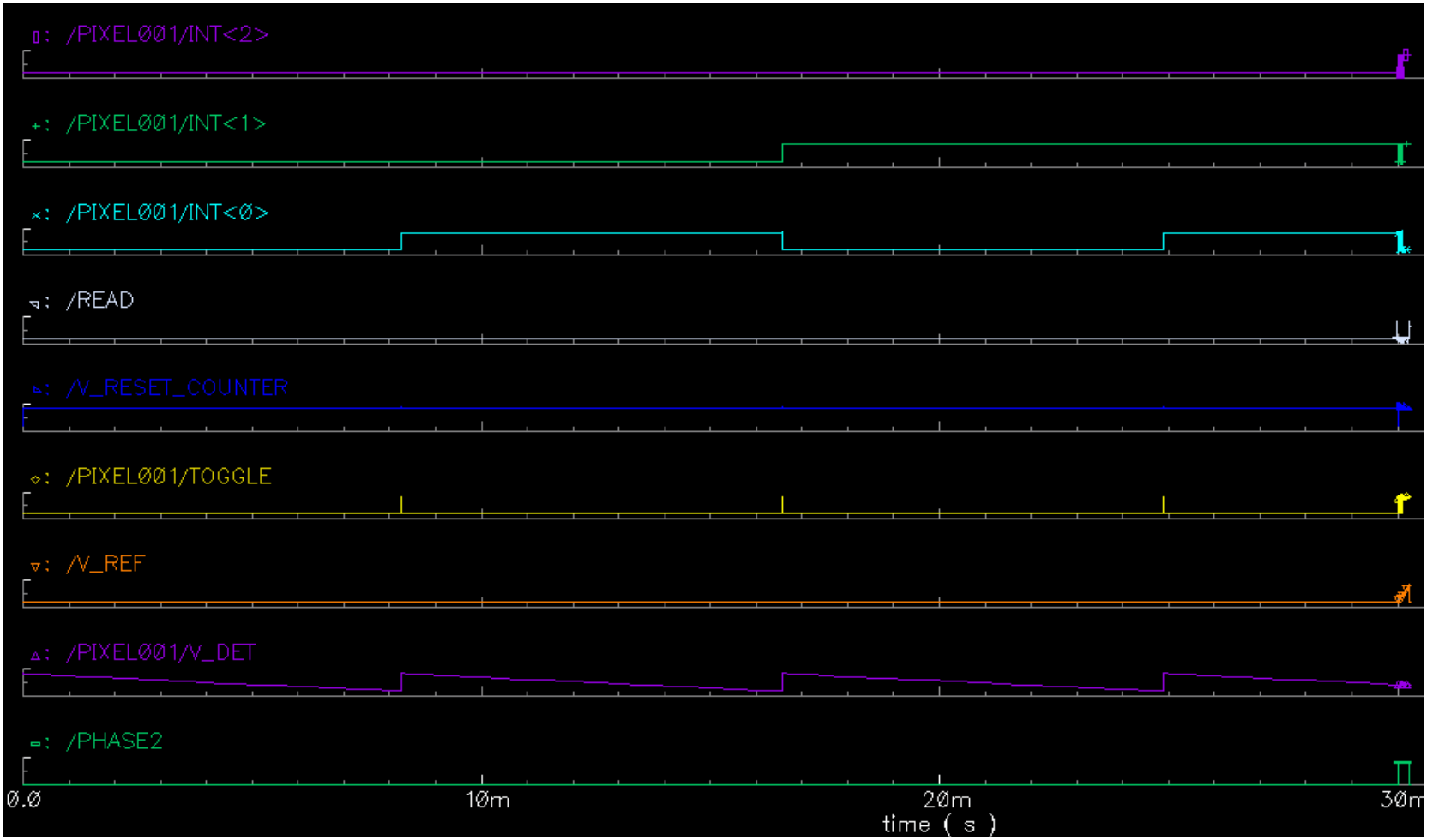
→ Comparator output goes high.

→ Counting is stopped (clock disconnected).

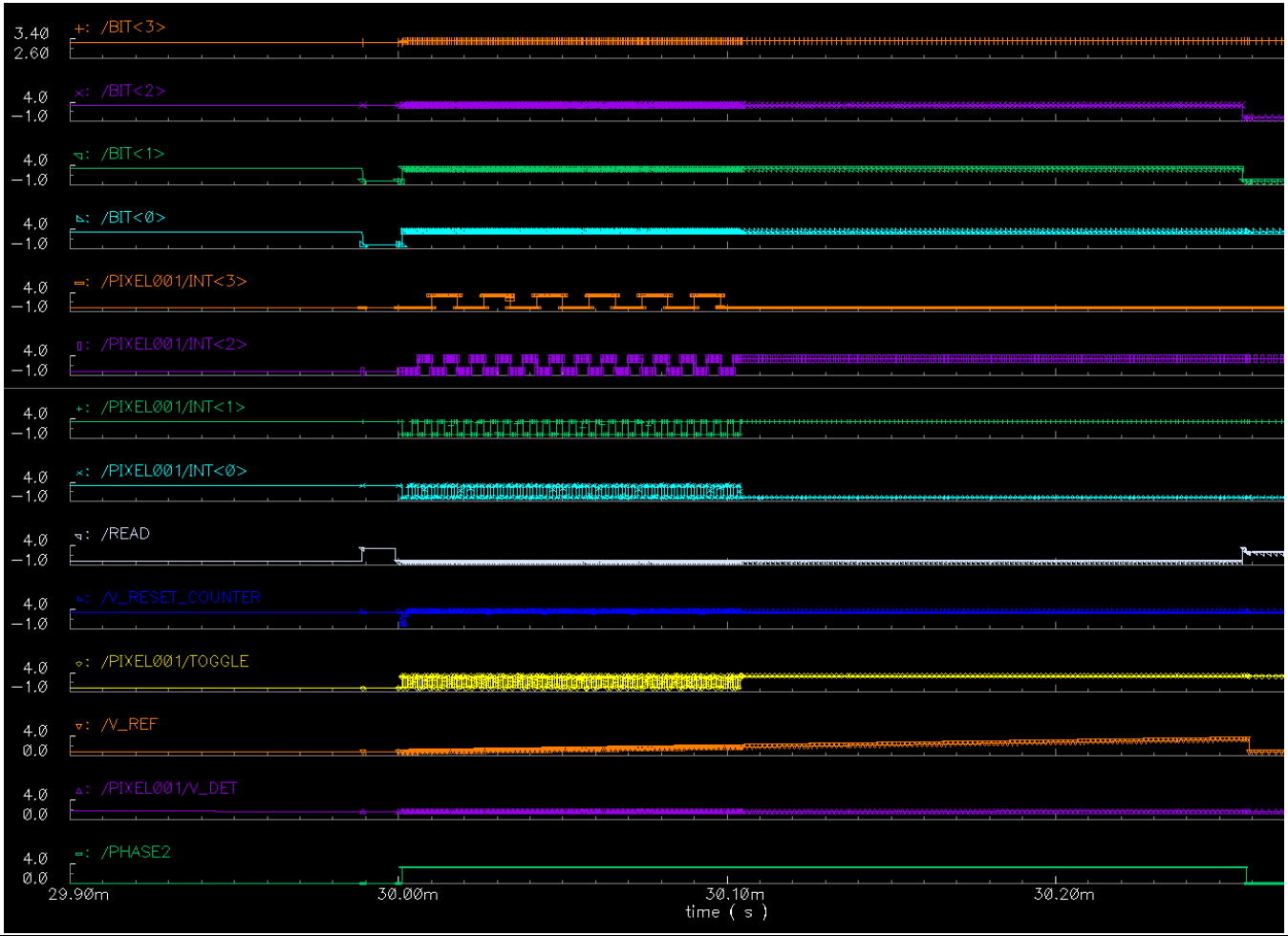
→ Writing to memory is enabled.



1. Self-Reset Technique



1. Self-Reset Technique



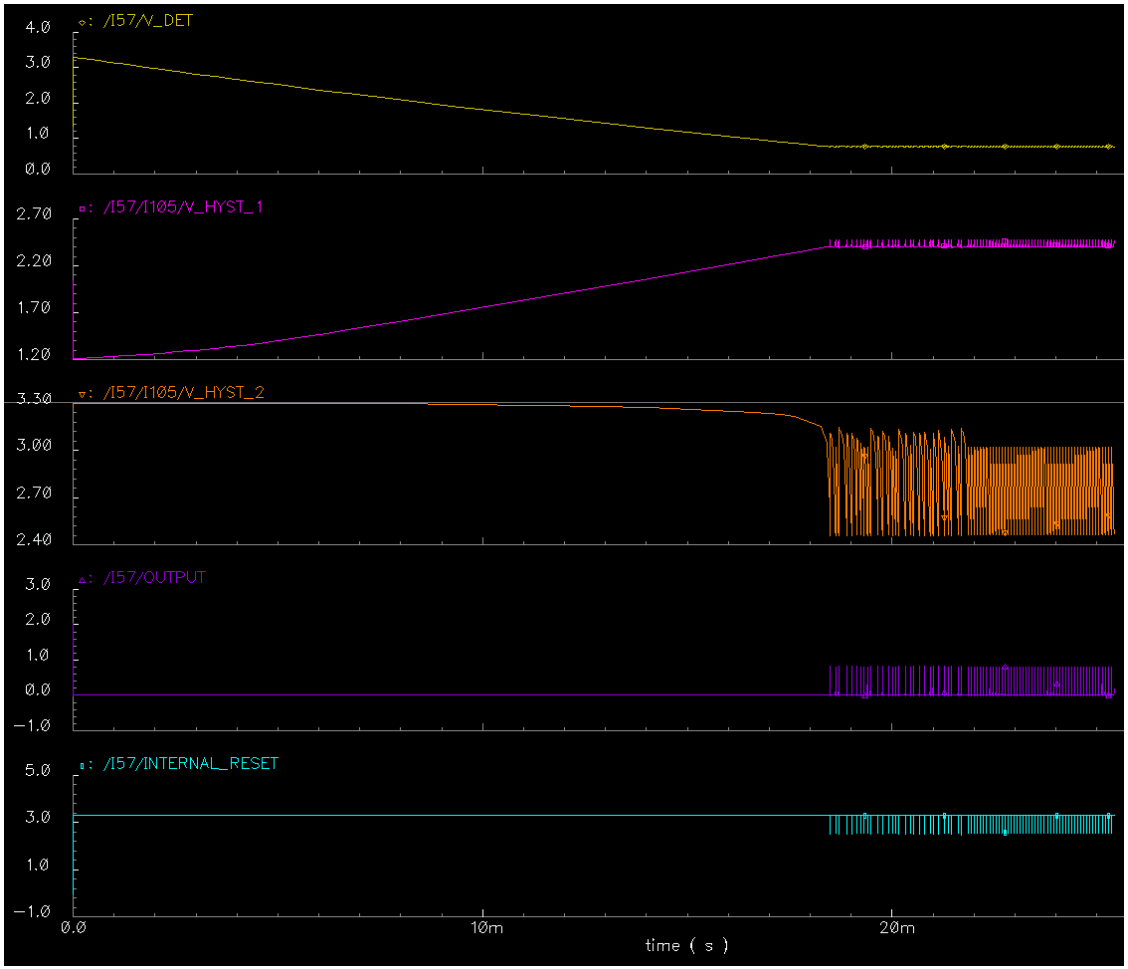
2. The Comparator

Design of the comparator will dominate the accuracy of the ADC conversion in phase 1 as well as in phase 2!

Requirements:

- Propagation delay as fast as possible.
- Very low offset voltage:
  - Auto-Zeroing applicable?
  - Reducing mismatch with layout techniques (common-centroid etc.).
  - Also important to **reduce the fixed pattern noise**.
- Proper quiescent point (not resetting the well in the first place).
- Low power consumption.
- **Further problem:**
  Comparator will start to oscillate especially on low light intensity!

2. The Comparator



Oscillation:

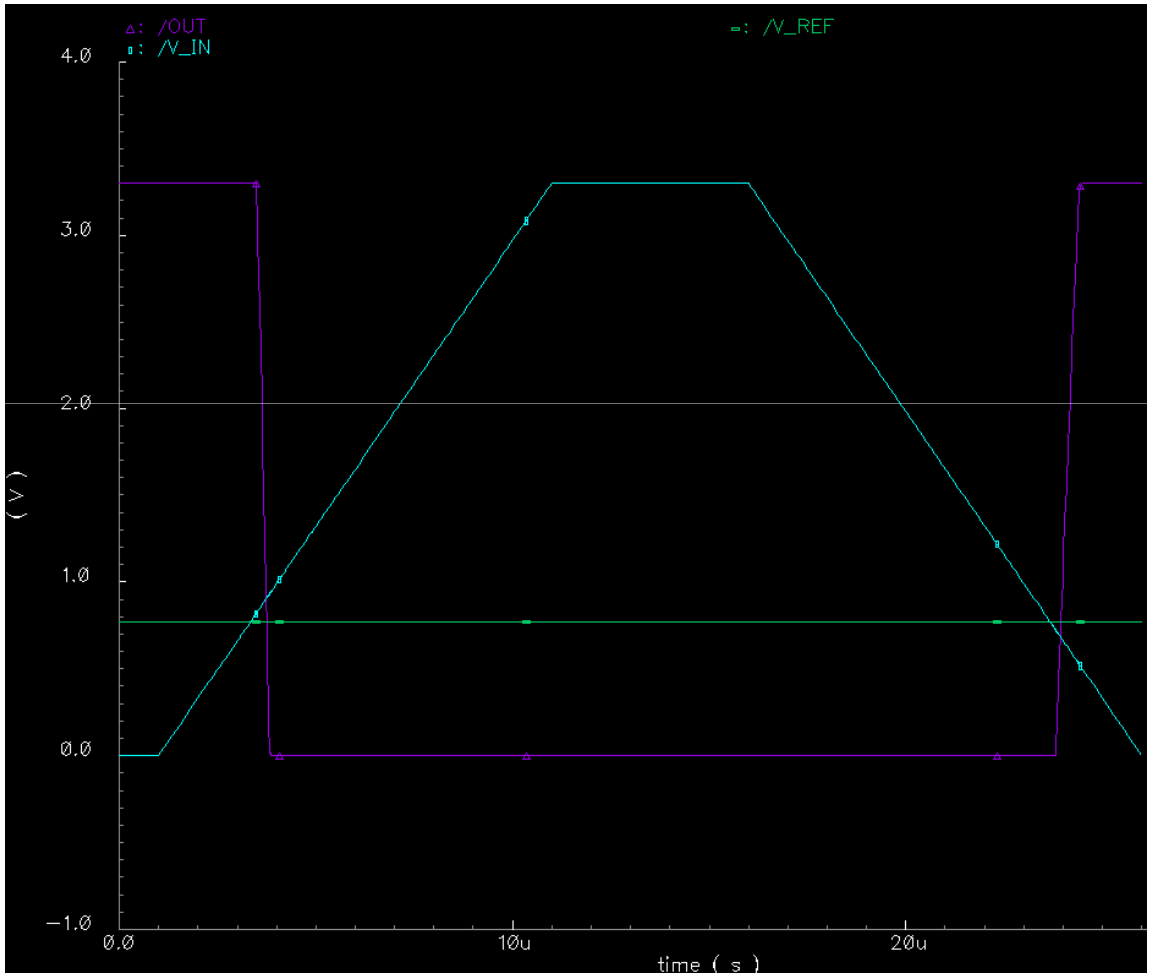
- Fast switching between reset and integration.
- Well is loaded for short time (subthreshold current)
- Detector Voltage reaches an equilibrium state.

→ No well reset possible!

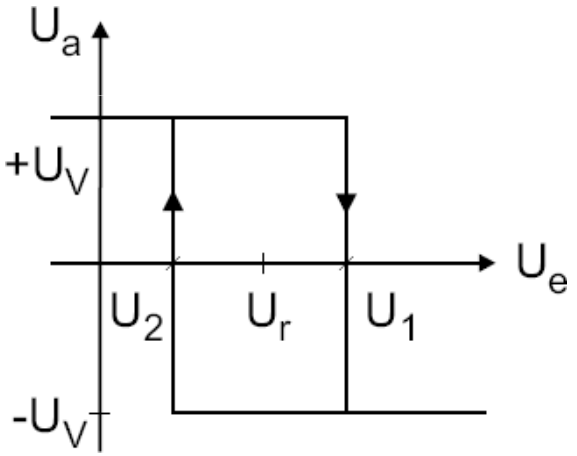
Solution:

Some kind of hysteresis has to be added to the comparator!

2. The Comparator



A Hysteresis of 20mV turned out to be sufficient to ensure correct operation.



→ Schmitt-Trigger

(different implementations possible)

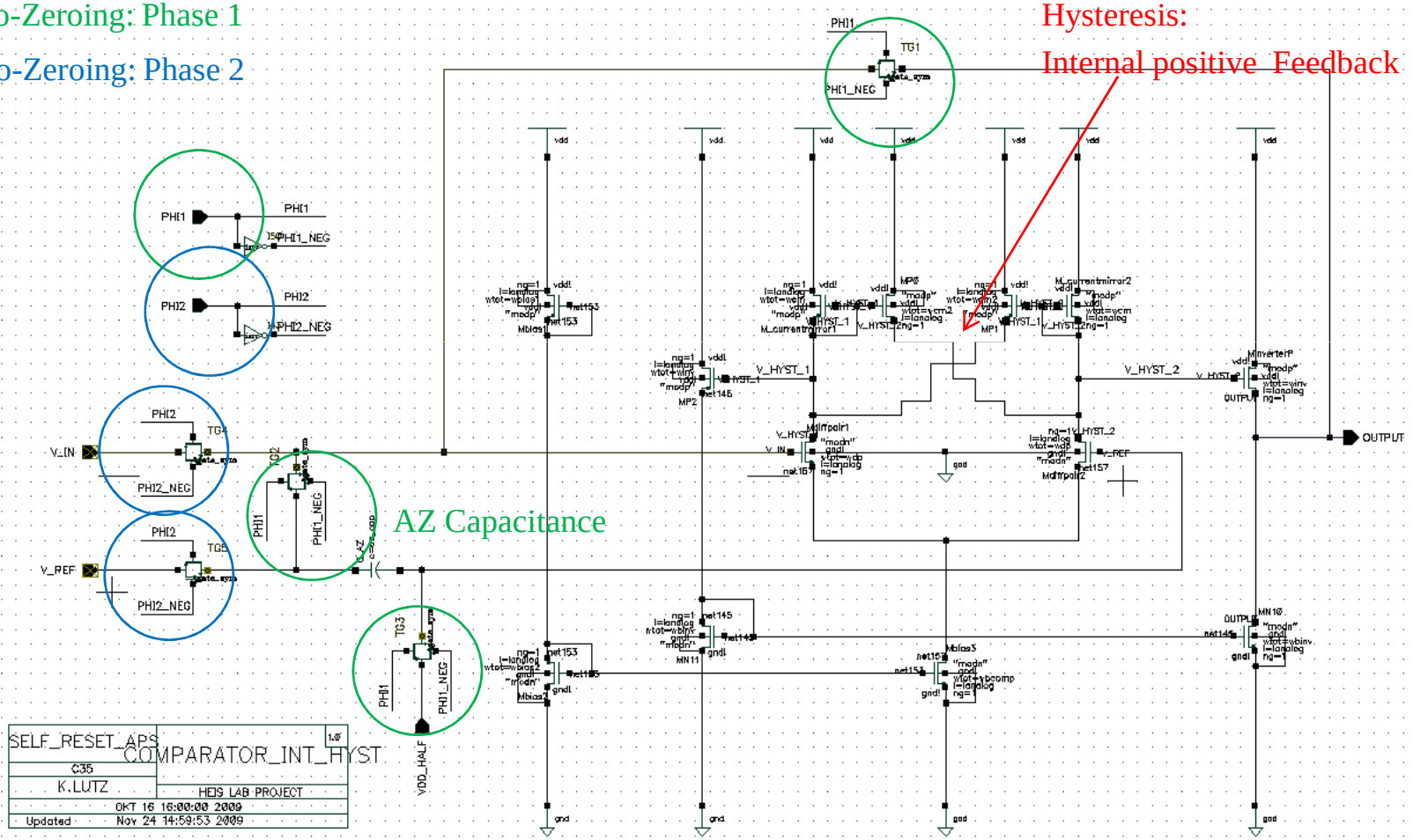
2. The Comparator

Auto-Zeroing: Phase 1

Auto-Zeroing: Phase 2

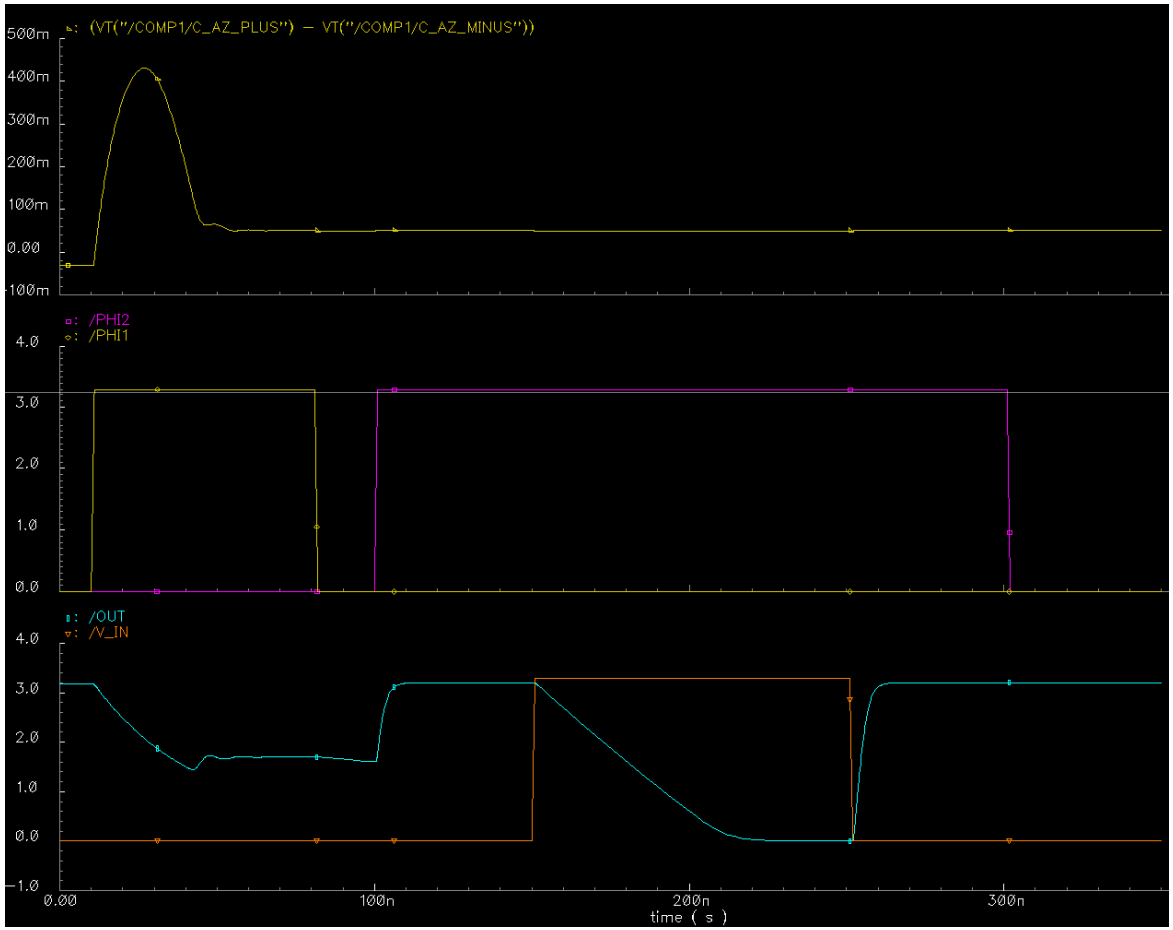
Hysteresis:

Internal positive Feedback



Autozeroing Example

- Also tendency to oscillation.
- Comparator needs to be compensated, or making the AZ-cap very high.
- Slows down the comp.



2. The Comparator

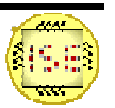
The problem with auto-zeroing:

- How to clock the auto-zeroing phases?
- Coarse ADC phase is asynchronous.
- Leakage current increases → falsifies the value in fine ADC.
- Worst case: Offset needs to be held on the transistor for 30ms (25frames/s)

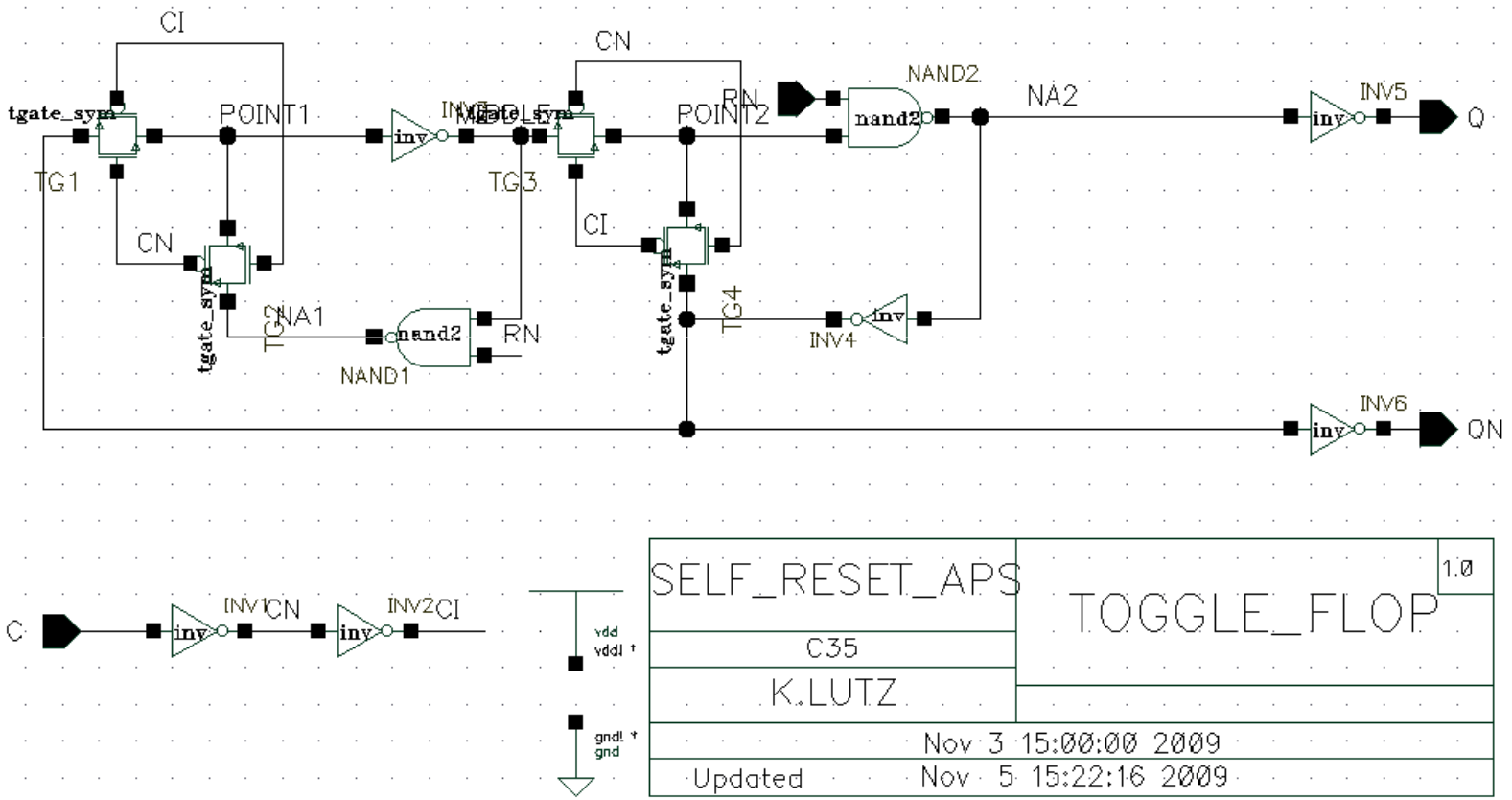
→ Capacitance will be enormous.

- AZ only simulated in schematic (with poor results).
- Final Layout will be without AZ → Layout techniques to reduce mismatch.

→ Deeper changes have to be made to make AZ applicable to the sensor.



3. Counter using toggle-FF‘s



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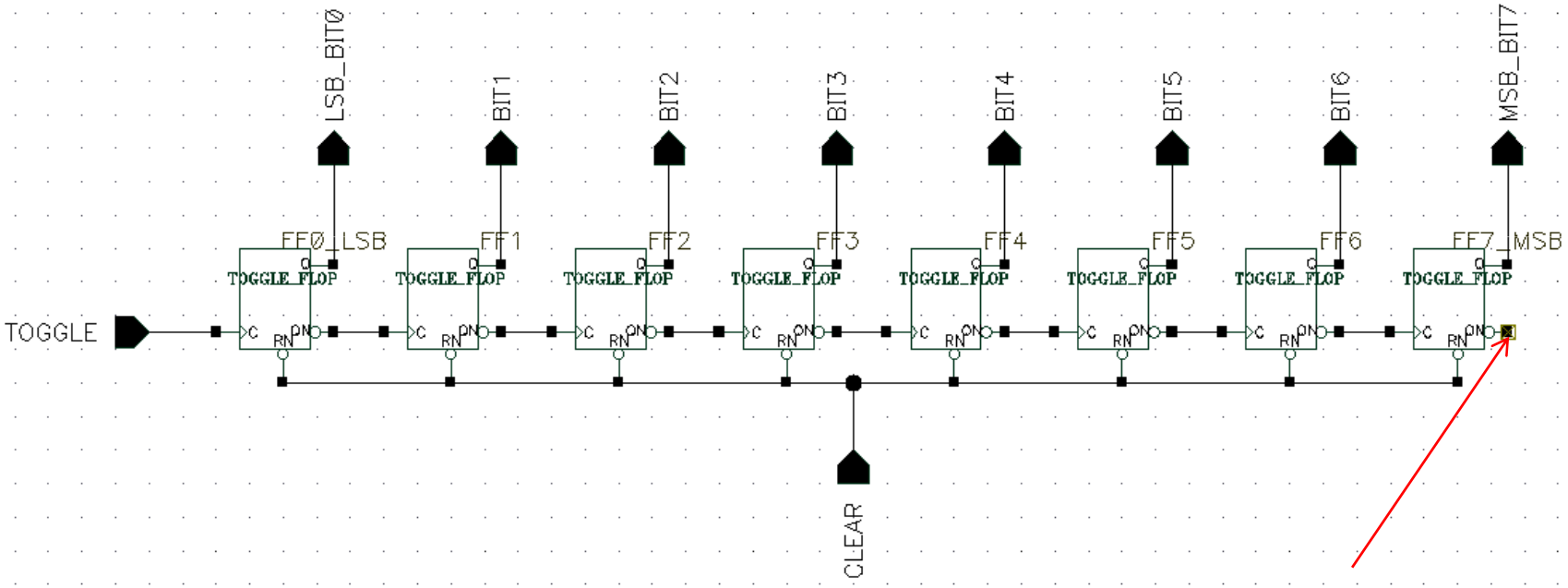
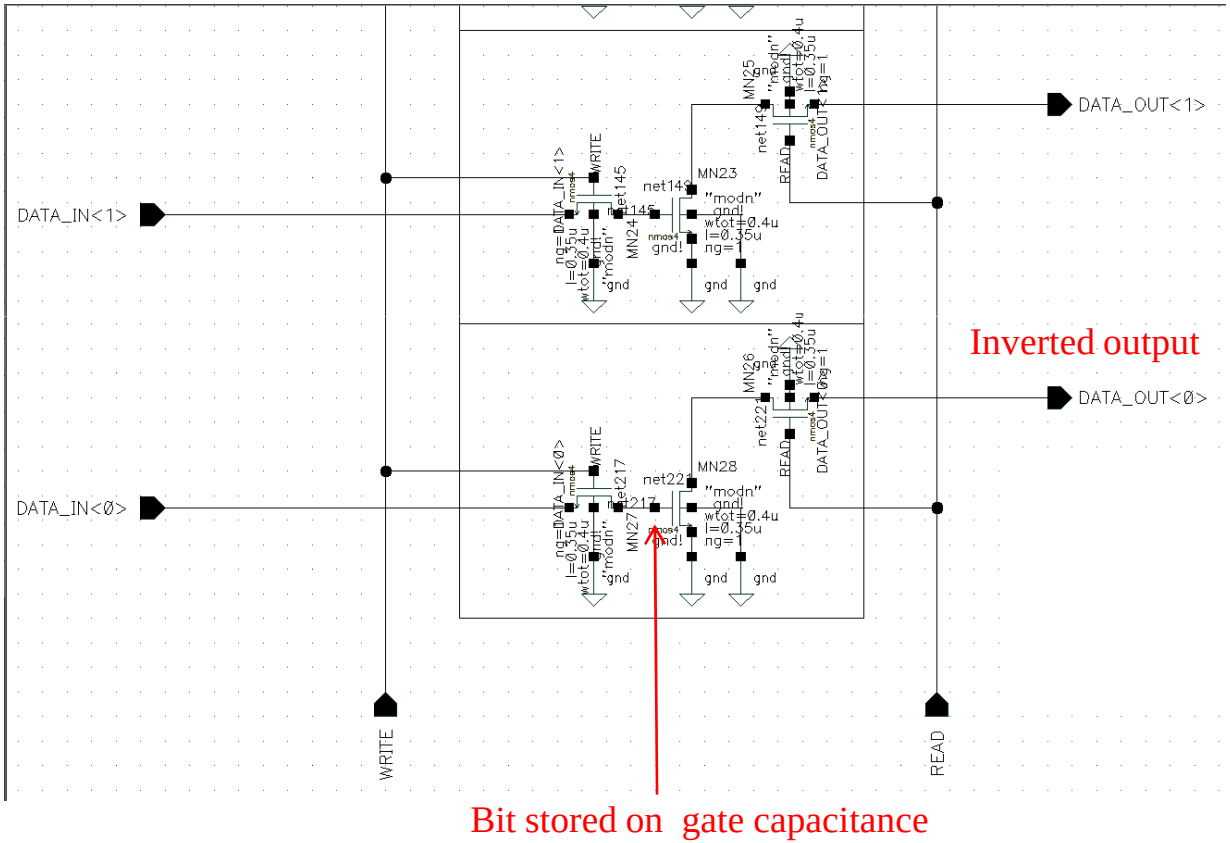


4. *4T DRAM Memory*



4th transistor is needed to precharge the DATA_OUT bits to high.

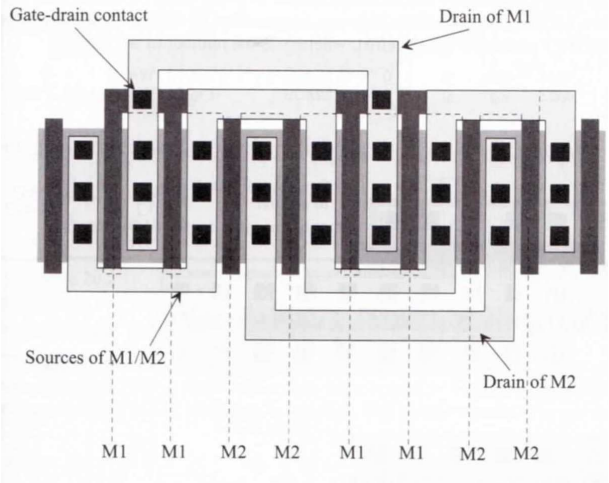
1. Global implementation:
Precharging the column bus for each row readout.

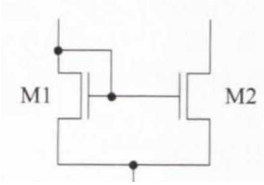
2. Local implementation:
Every bit needs its own precharge transistor.

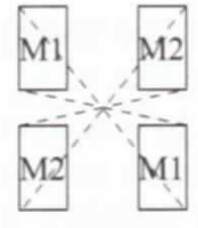
Trade-off in driving strength.
Speed vs. Power consumption

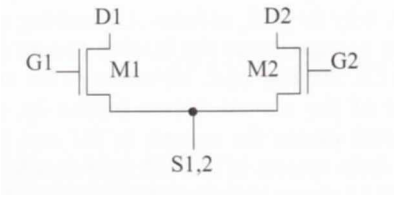
5. Layout

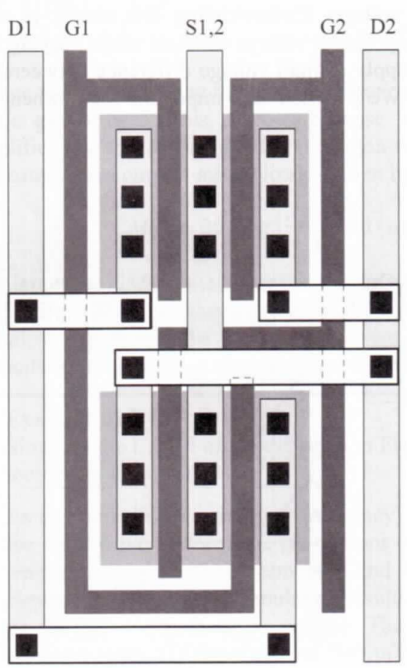
- Apply matching techniques to avoid missmatch.
- Common centroid layout to take out manufacturing gradients in both directions.
- Length of analog part has increased to 1µm to suffer less from channel length modulation. Digital parts have (mostly) minimum dimensions.
- Dummy transistors, or dummy stripes at the end of rows.
- Separate digital and analog part.
- Shielding of the diode to avoid blooming.



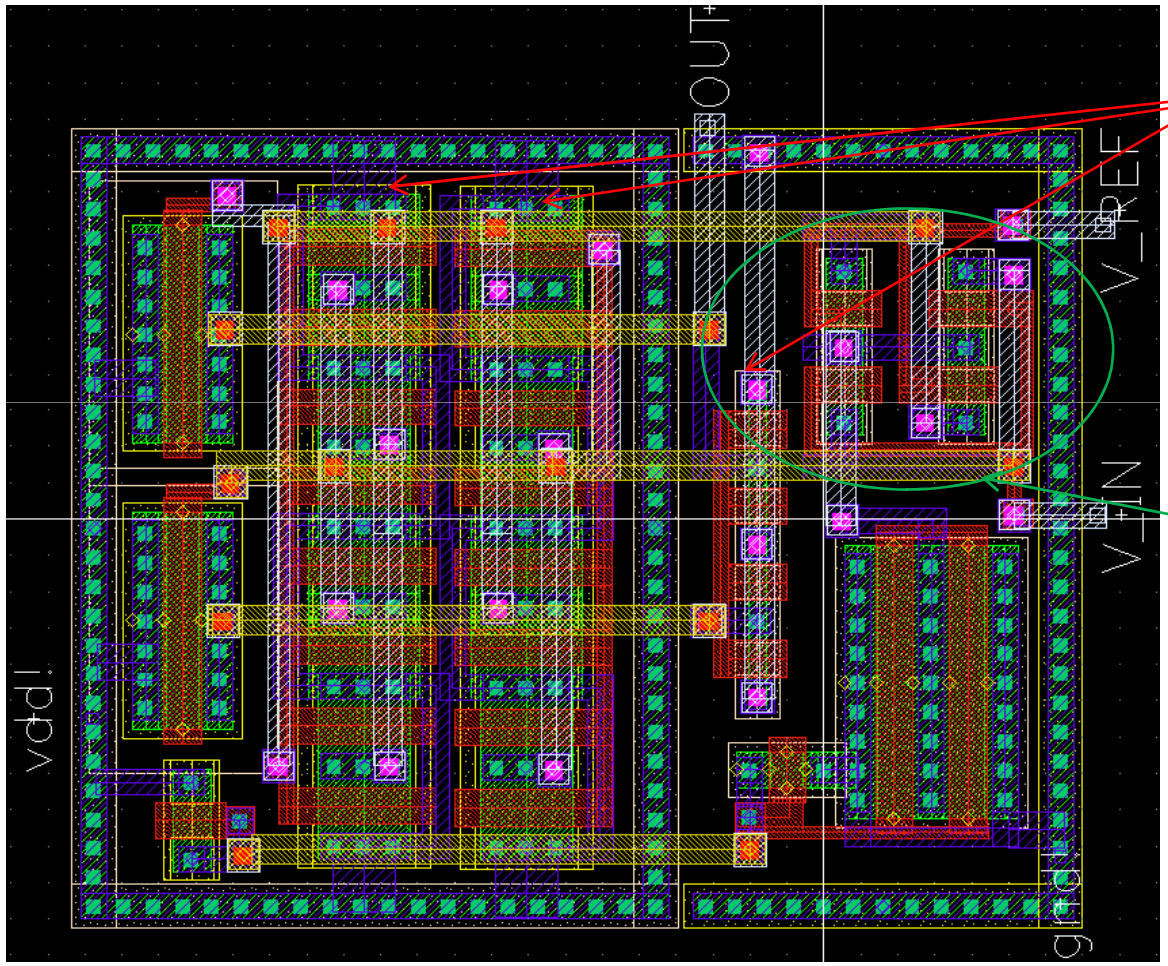








5. Layout: Comparator



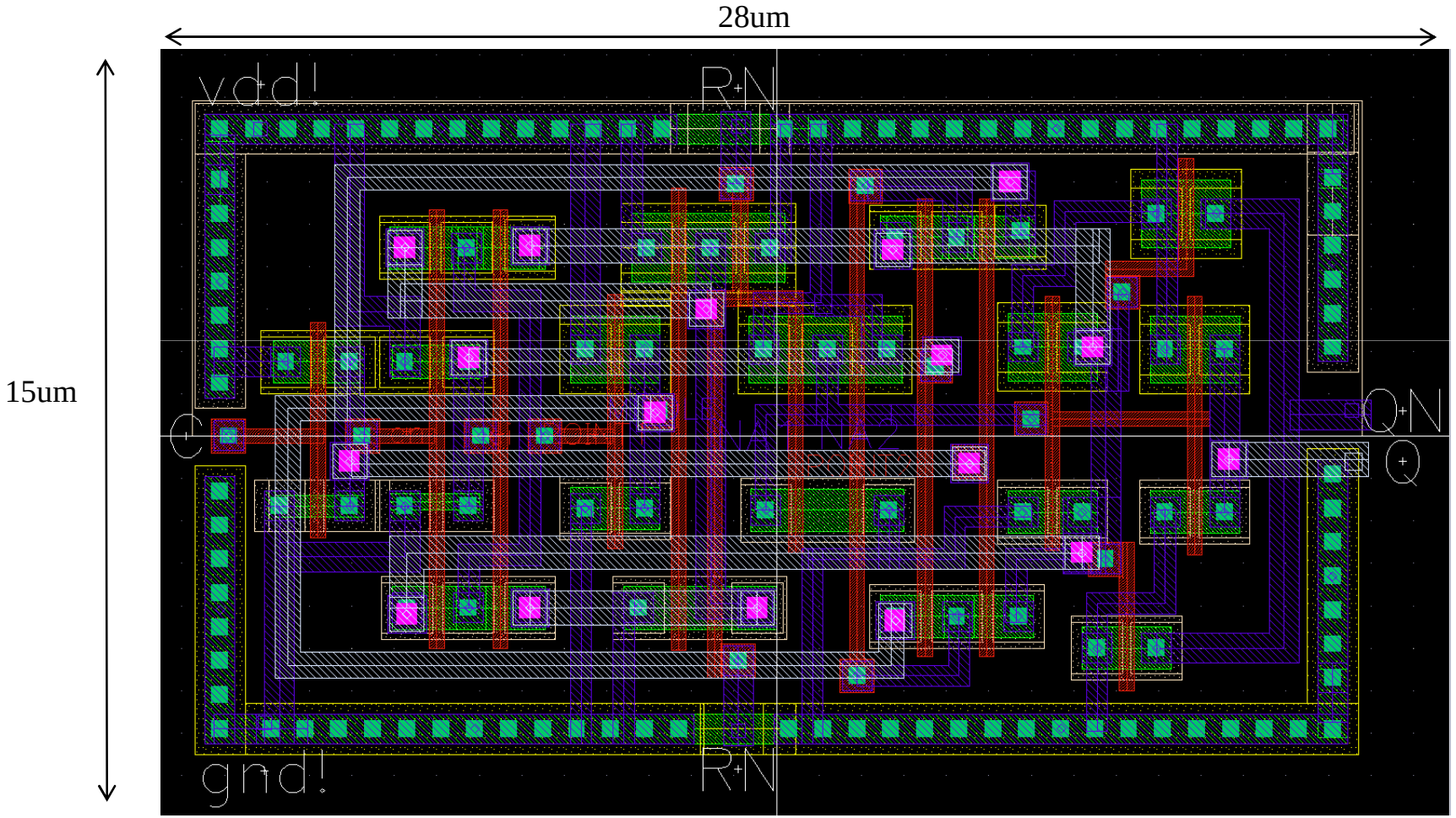
20um

Dummy stripes missing

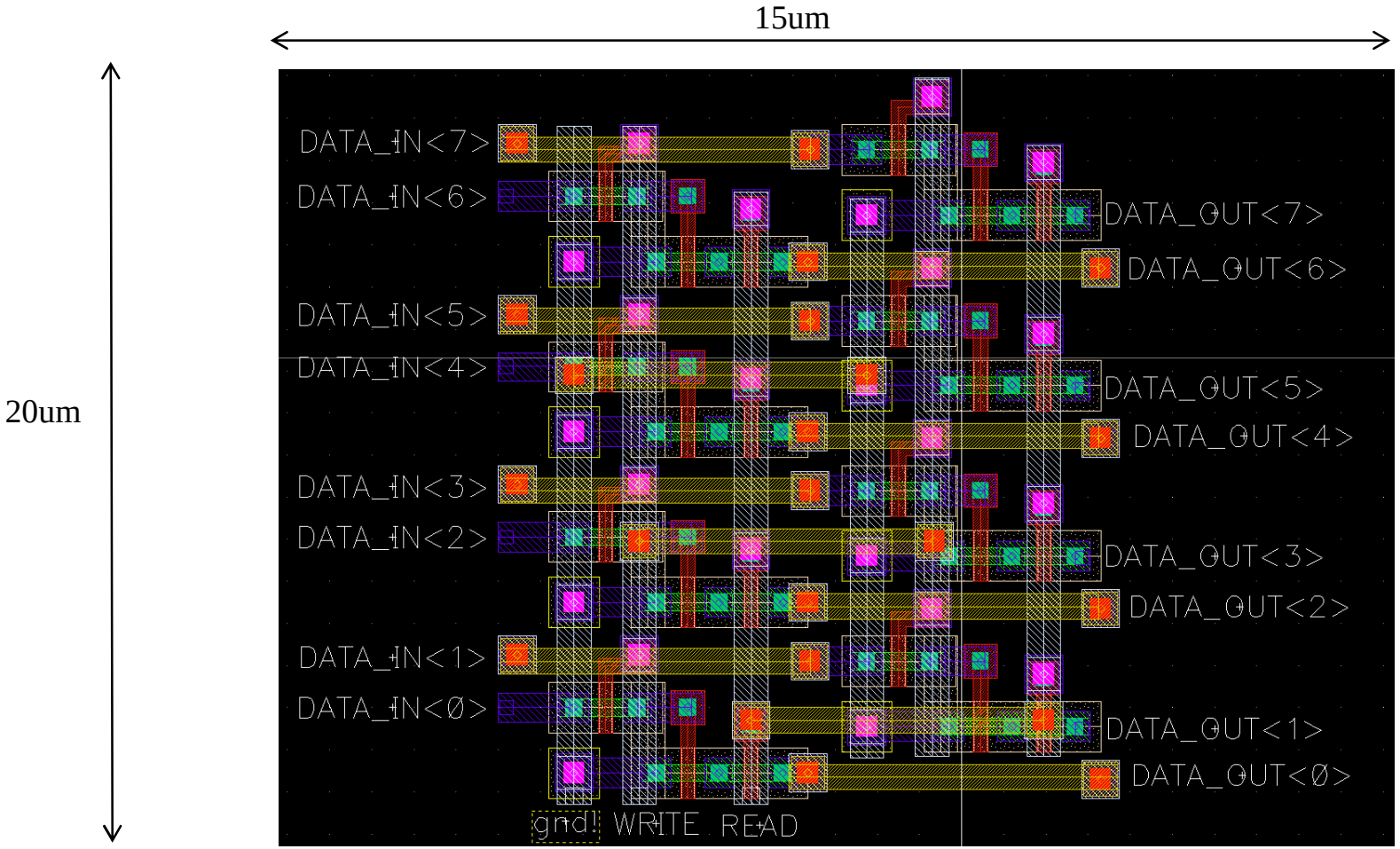
Common centroid diffpair

Well contacts surround nwell
(Guard Ring)

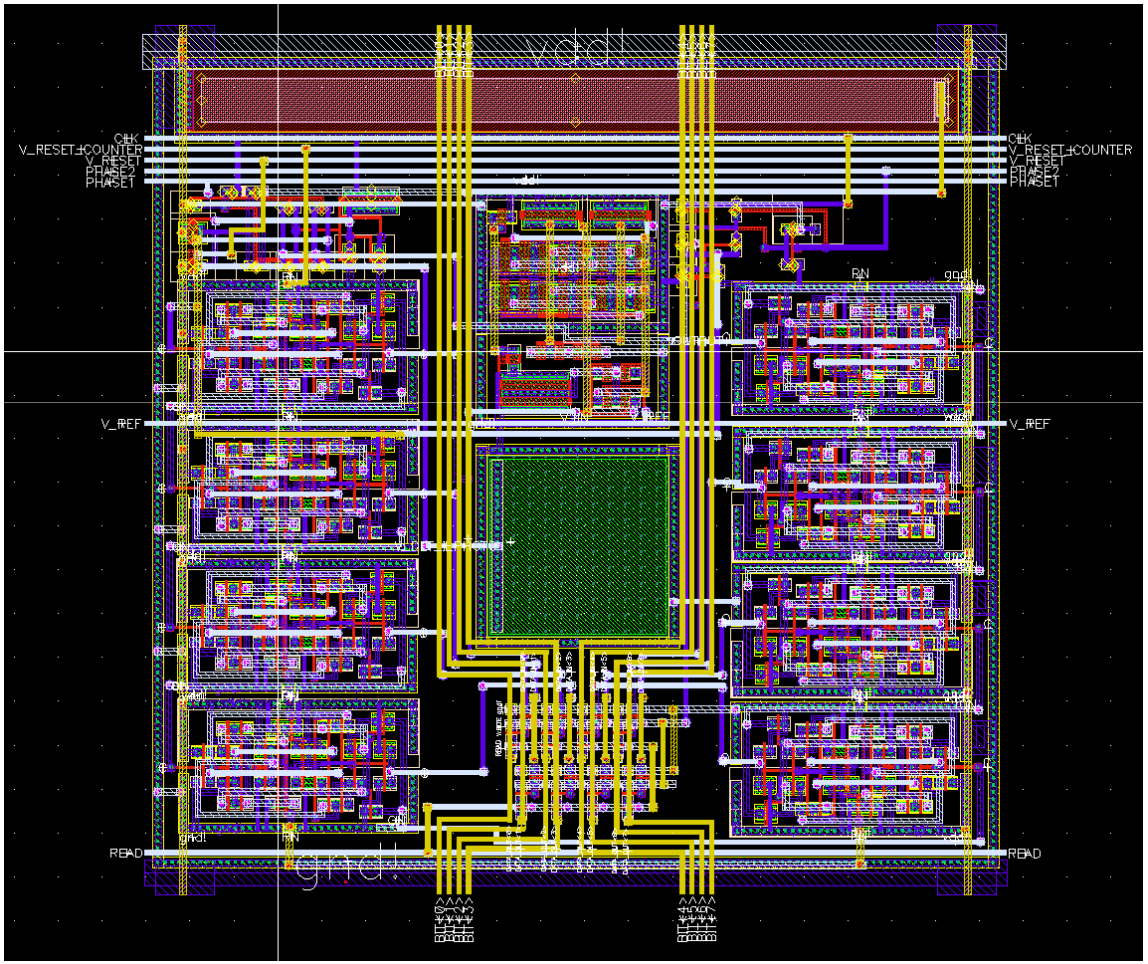
5. Layout: Toggle FF



5. Layout: 8 Bit Memory Cell



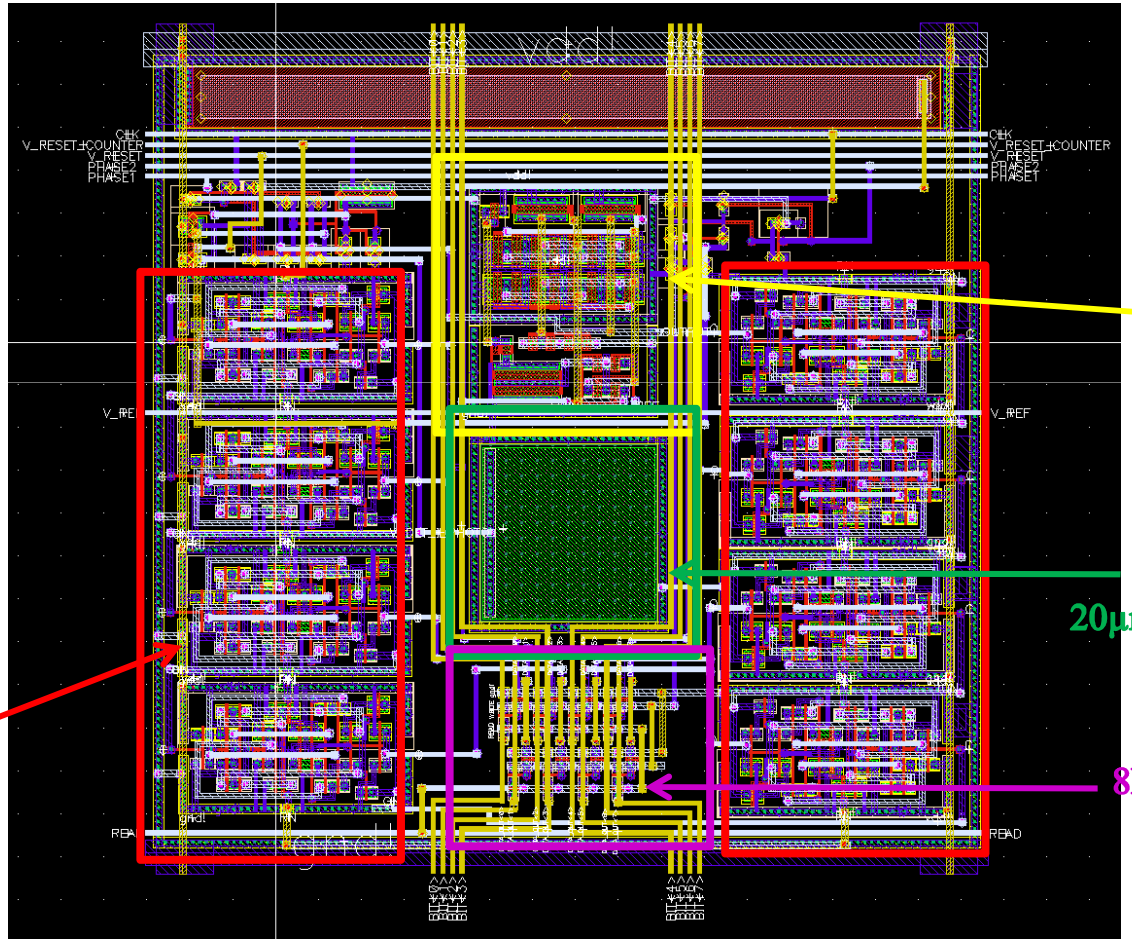
5. Layout



≈ 90µm

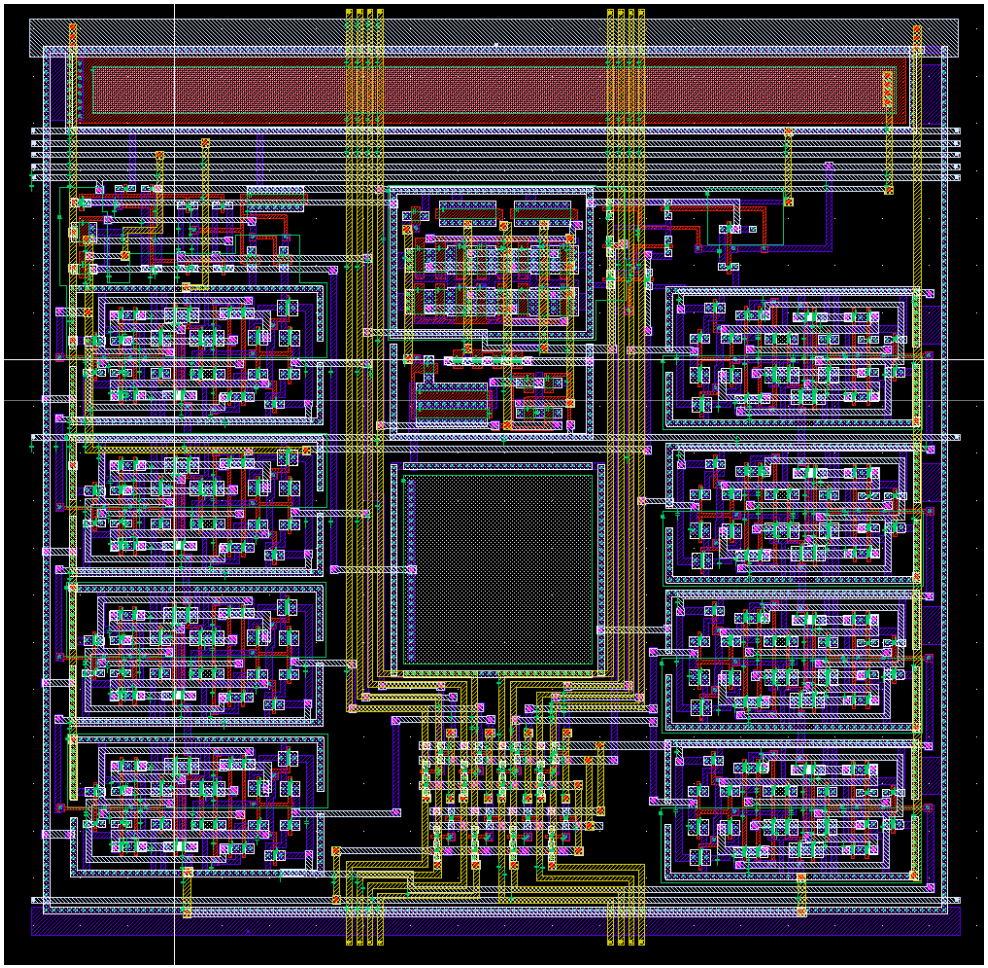
Fill Factor ≈ 5%

5. Layout



5. Layout

Extracted view:



5. Layout – LVS

/exp

File

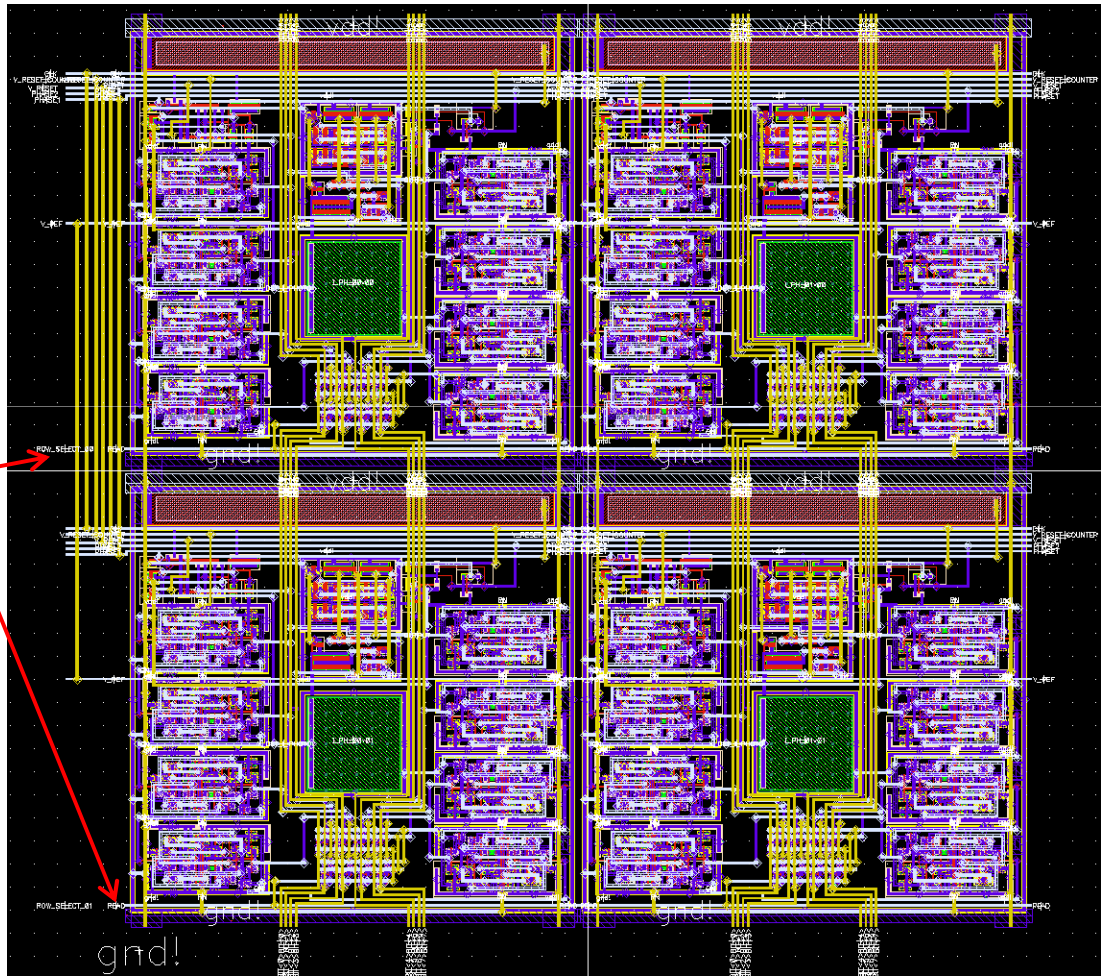
```
@(#)$CDS: LVS version 5.0.0 05/30/2003 19:44 (cds11939) $

Like matching is enabled.
Net swapping is enabled.
Fixed device checking is enabled.
Using terminal names as correspondence points.
 Permute MOS option disabled.

    Net-list summary for /export/users/sens5/LVS/layout/netlist
       count
         144            nets
          18            terminals
         156            rmos4
           1            cpoly
         143            pmos4
           1            nd

    Net-list summary for /export/users/sens5/LVS/schematic/netlist
       count
         144            nets
          18            terminals
         151            rmos4
           1            cpoly
         131            pmos4
           1            nd


    Terminal correspondence points
           1     BIT<0>
           2     BIT<1>
           3     BIT<2>
           4     BIT<3>
           5     BIT<4>
           6     BIT<5>
           7     BIT<6>
           8     BIT<7>
           9     CLK
          10     PHASE1
          11     PHASE2
          12     READ
          13     V_DET_I_PHOTO
          14     V_REF
          15     V_RESET
          16     V_RESET_COUNTER
          17     gnd!
          18     vdd!
```

```
The net-lists match.

                              layout  schematic
                                 instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   301     284
        total                    301     284

                                   nets
        un-matched               0       0
        merged                   0       0
        pruned                   0       0
        active                   144     144
        total                    144     144

                                 terminals
        un-matched               0       0
        matched but
        different type           0       0
        total                    18      18


Probe files from /export/users/sens5/LVS/schematic

devbad.out:
```

5. Layout

Matrix layout :

- Easy placement .
- No routing channels needed.
- Input signals (clk, v_ref, etc.) connected from the left.
- Column bus from top to bottom, routed inside the cell.
- Row_Select signals connect and disconnect the outputs to the column bus.
- Column busses will be read out with e.g. shift register.



6. Simulation Results

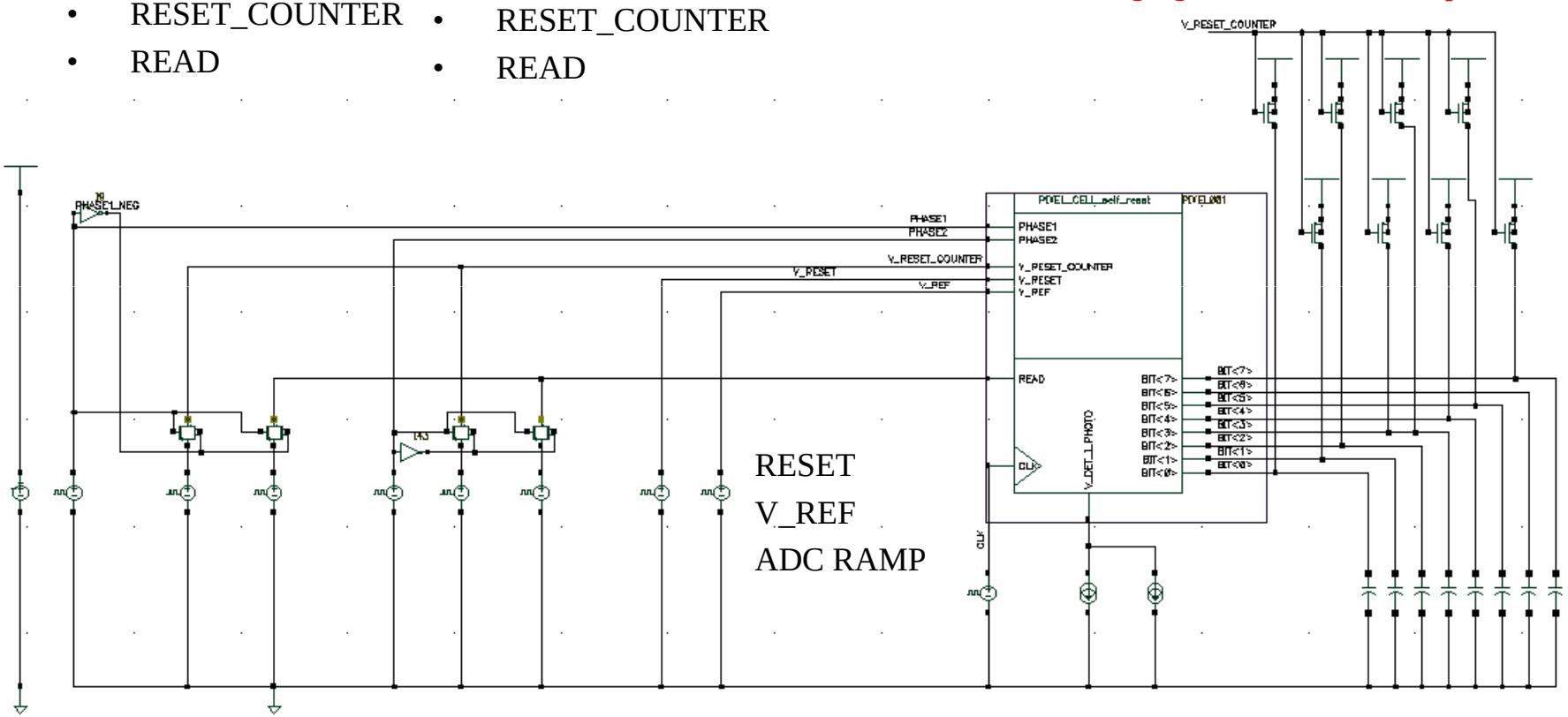
Phase1:

- RESET_COUNTER
- READ

Phase2:

- RESET_COUNTER
- READ

Precharging: Done outside the pixel cell



CLK and artificial photo current

6. Simulation Results

- Photo diode with 20µm* 20µm. Pixel Cell≈ 90µm* 90µm

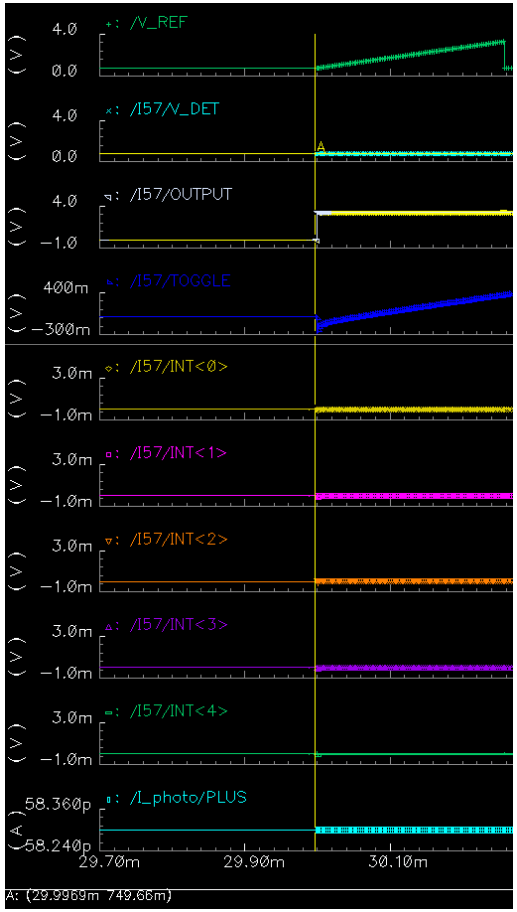
→ Fill Factor ≈ 5%

- Dark current ≈ 4fA.
- Resetting the well to Vdd (3.3v).
- Integrating down to 750mV .
- Integration time 30ms (10ms for reserved for readout → 25 frames/s)
- 2.55V with a resolution of 8bit → 0.01V per step.
- Ramp raise time of 255µs.
- Clock period time of 1µs.
- Dynamic Range ≈ 100dB (200fA – 20nA photocurrent) - Normal APS ≈ 60dB

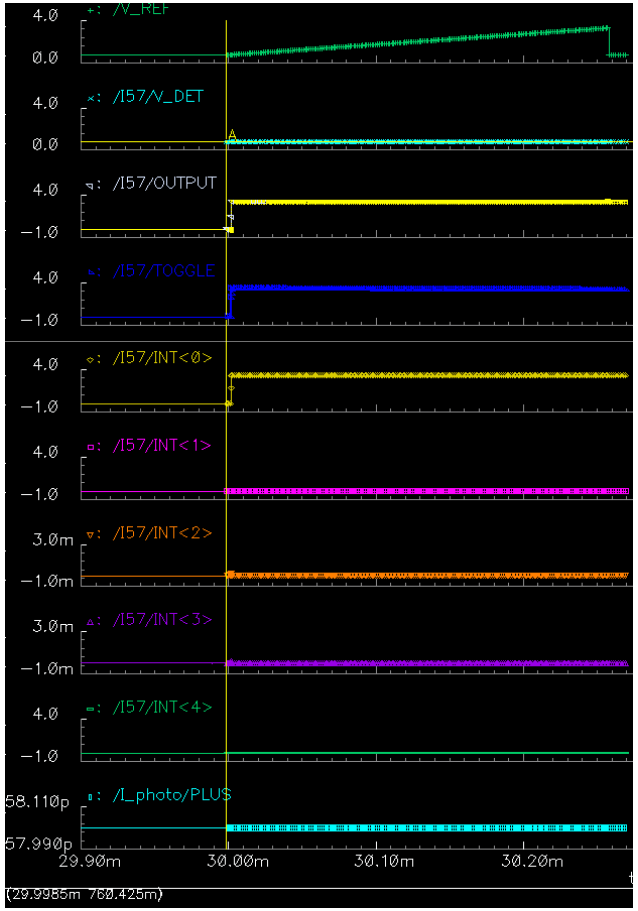
$$DR(dB) = 20\log\left(\frac{20\times10^{-9}}{200\times10^{-15}}\right) = 20\log(10^{5}) = 100dB$$

6. Simulation Results

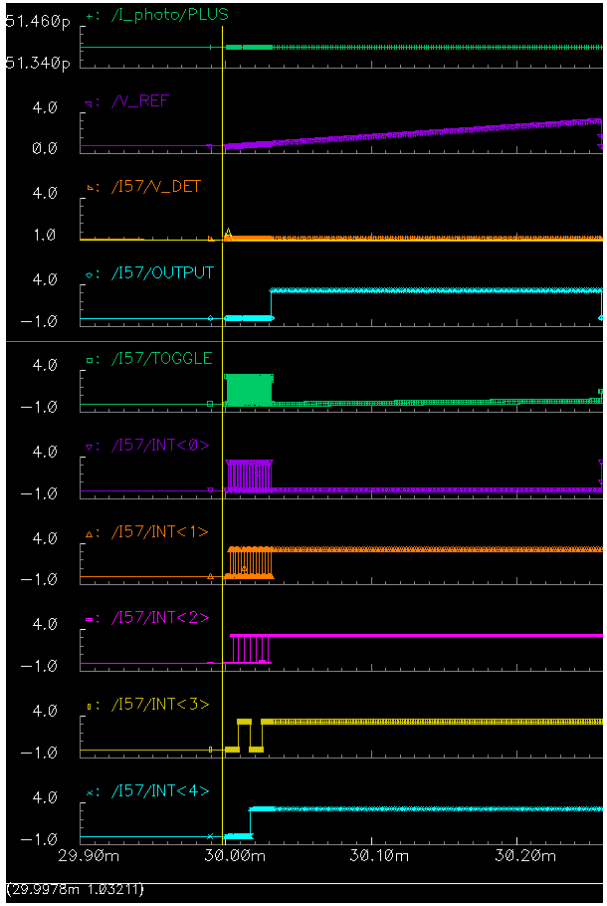
Max. current before reset: 255



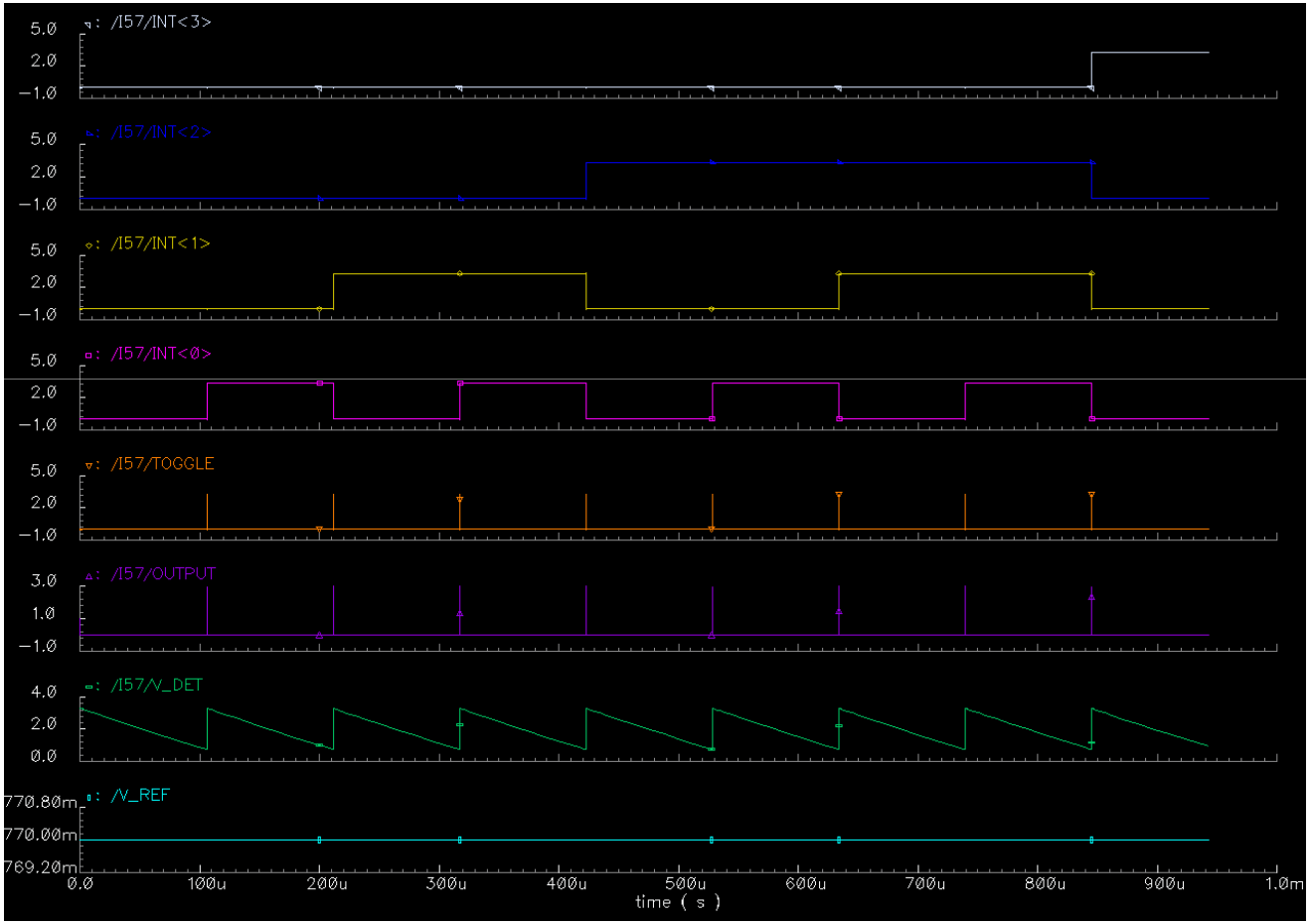
Decrease current: 760mV → 254



Further decrease : 1.05V → 225



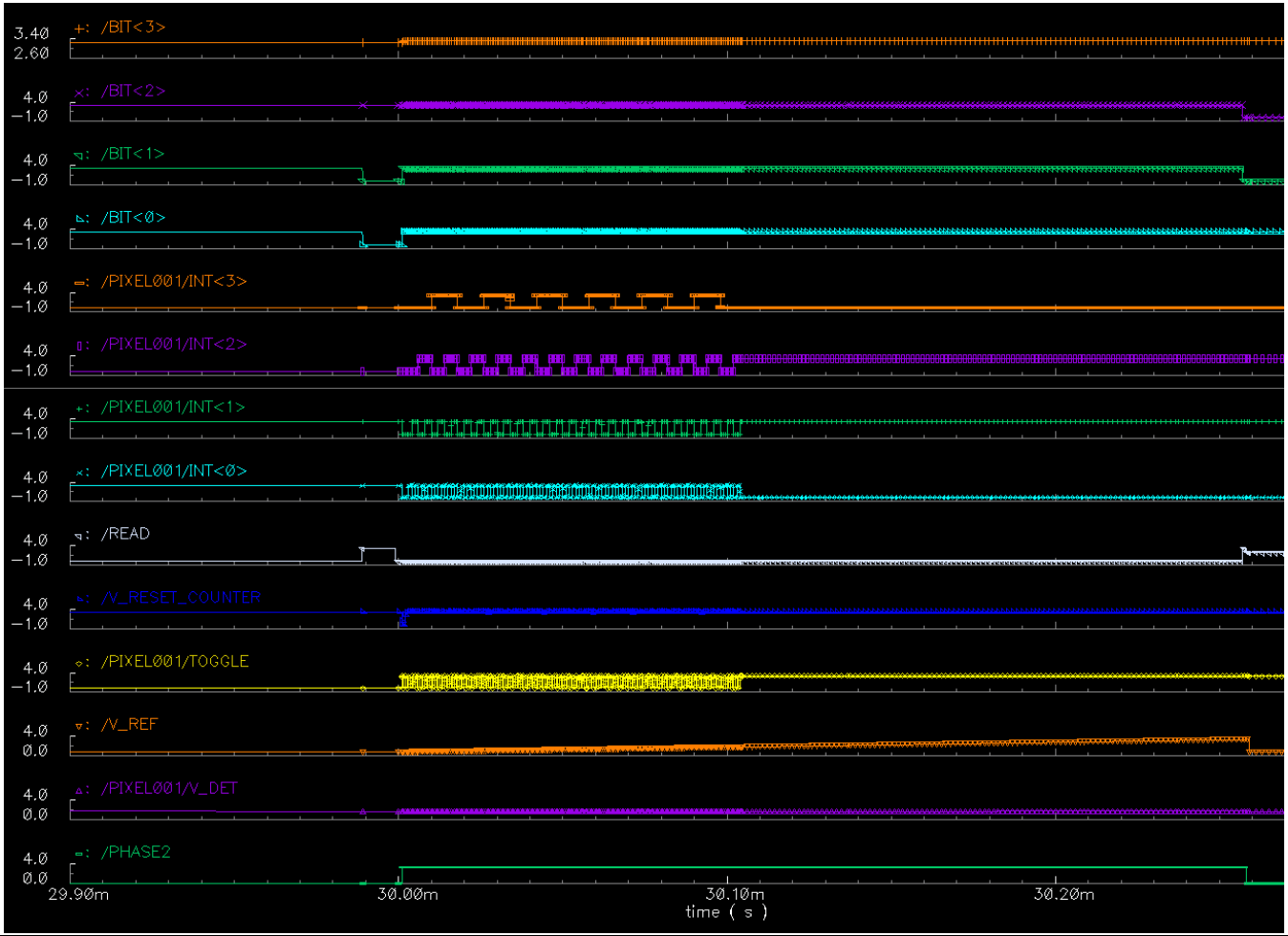
6. Simulation Results



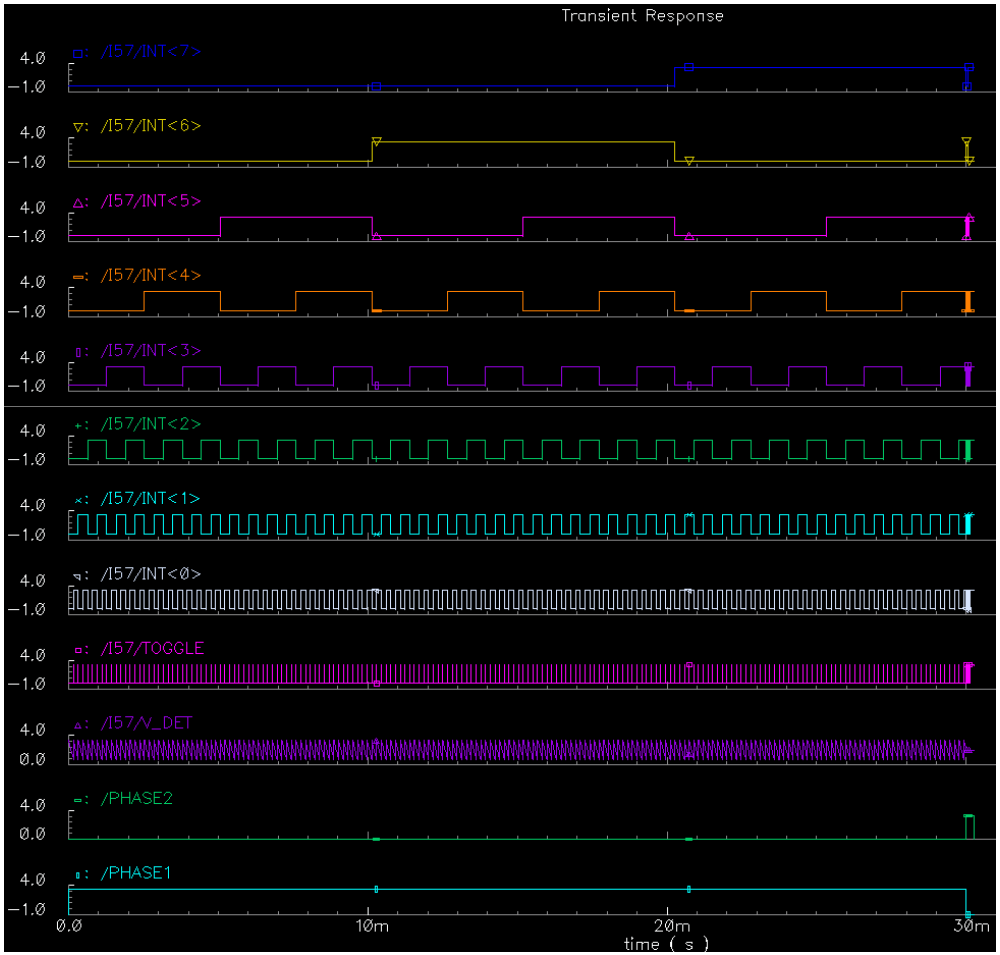
- Maximum detectable current ≈ 20nA
- 30ms integration

≈ 100us between each resets.

6. Simulation Results

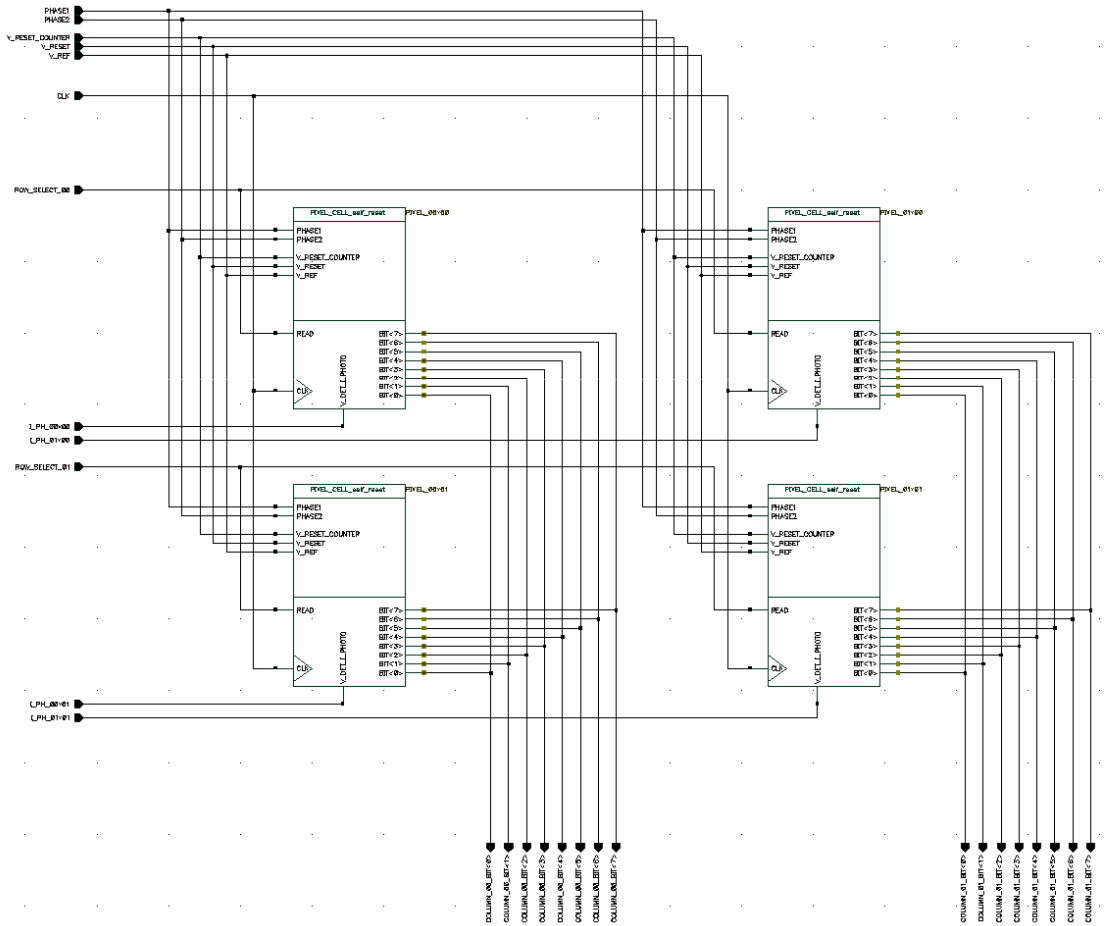


6. Simulation Results



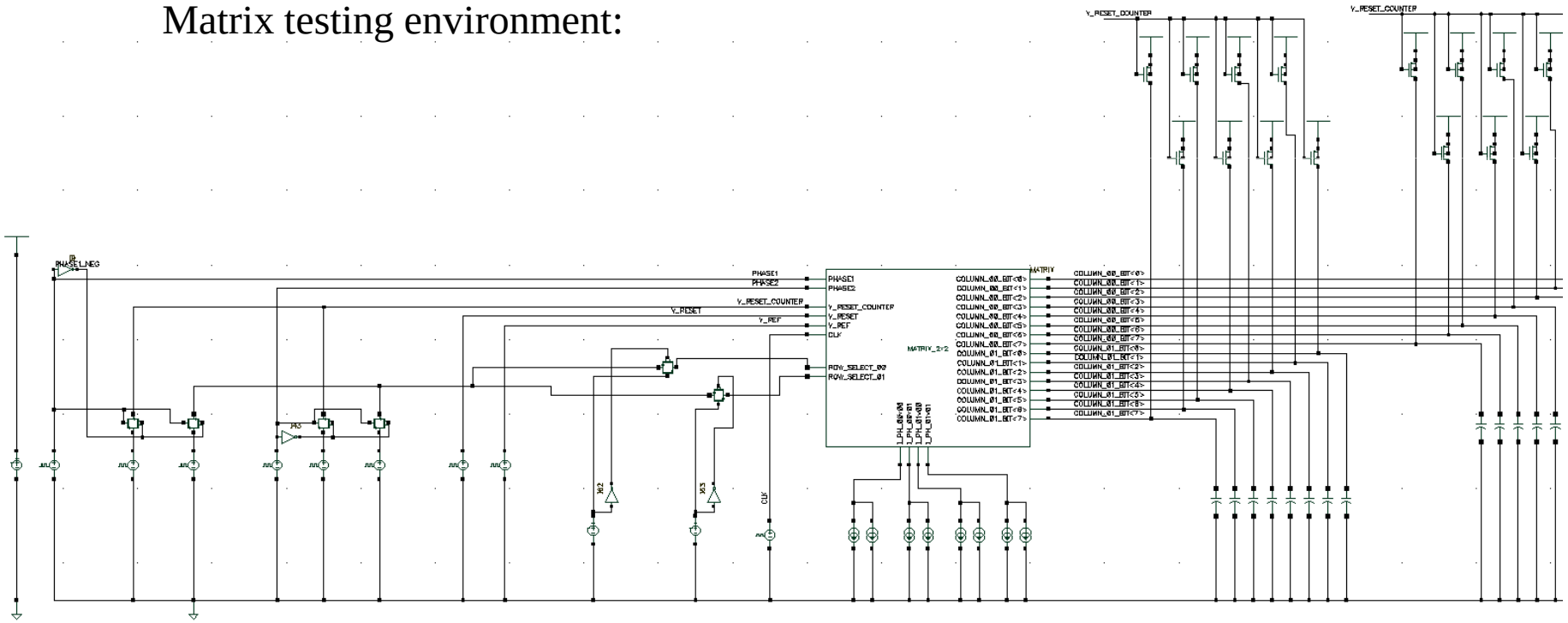
6. Simulation Results

Schematic of the matrix:



6. Simulation Results

Matrix testing environment:

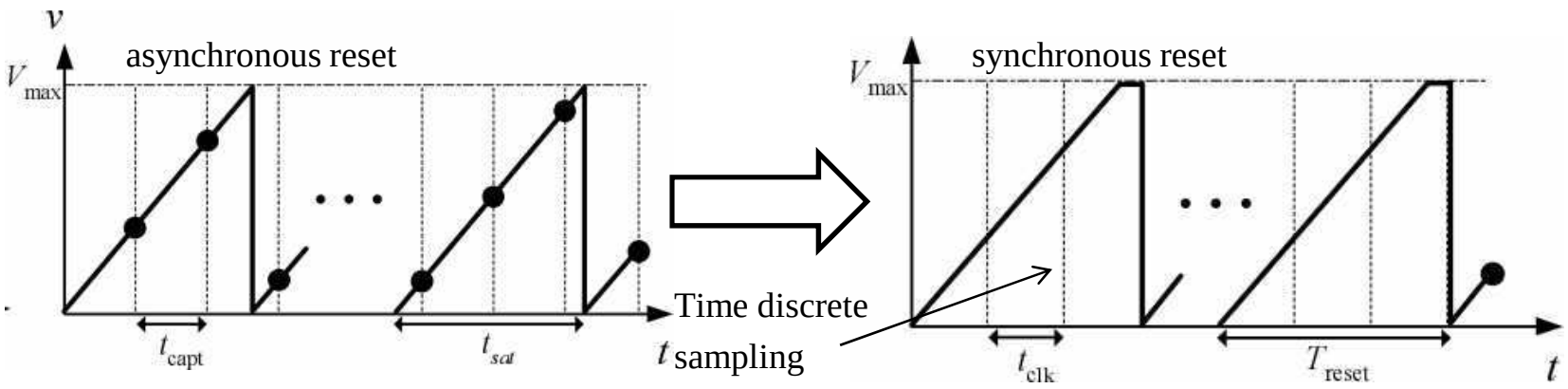


Conclusion and Future Work

- Dynamic range is increased at the cost of dramatically decreased fill factor and an increase in power consumption and complexity!
- SNR improvement makes this technique preferable over the others.
- Hysteresis is important to ensure proper operation.
- Many sources of mismatch resulting in increased FPN remain. Matching is very important when it comes to the layout.
- To apply auto-zeroing to the sensor, the offset needs to be stored in different ways (DAC) or the ADC conversion scheme has to be changed to make the behavior more predictable or synchronous.
- Readout and precharge cycles will be time and energy consuming. Maximal frame rate should be determined (Rhee,Joo up to 1000 frames/s)

Conclusion and Future Work

- Readout scheme has to be developed
  - 8bit coarse ADC and 8bit fine ADC.
- Investigate time discrete operation with photocurrent estimation [9].
- Reinvestigate solutions to apply auto-zeroing:
  - Add 3. phase with offset readout – store in outside memory and add/sub later from measured values.
  - Make resets synchronous (see. [1][9]).



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The End

Thank you for your attention!

Questions?